QUELE

Wed, 2012-03-28 12:54 - Lukas Theussl **Full Name:** Quantum computing with trapped electrons
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Location

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Website:
http://fisica.unicam.it/quele/

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Following our successful assessment project QUELE, we aim with the present proposal at building and operating a universal scalable quantum processor consisting of 3-10 trapped electrons. Confinement will be performed in a Penning trap using a new concept of planar geometry. Ultra-high vacuum conditions will minimize the effect of the environment. The use of static fields is an advantage over rf ion traps because of weaker decoherence effects due to the absence of r.f. heating.

The accomplishment of the final task requires a number of theoretical and experimental intermediate steps:
- Design, set-up, and operation of a highly innovative multi-electron planar trap;
- Cooling of the electron motion via mode coupling between the cyclotron and axial oscillator;
- Single particle addressability by adjusting the voltage applied to the trap electrodes and introducing a small magnetic field gradient;
- Initialization to a fiducial state of the qubits, encoded in the electron spin and in the quantized external degrees of freedom (axial and cyclotron oscillators);
- To develop the microwave and radio-frequency sources required in one- and two-qubit operations on a single electron;
- Realization of two-qubit operations on different electrons via the controlled Coulomb interaction, switching on and off resonance any two axial oscillators, by image charge coupling;
- To understand the decoherence processes and estimate the relevant decoherence rates, taking into account intrinsic (thermal) and technical noise sources;
- To characterize the performances of our prototype of quantum computer in terms of achievable fidelity and clock speed;
- To devise and implement a strategy for measuring the final state of individual qubits.

With our original prototype of quantum processor we expect to experimentally validate some quantum algorithms, to implement error correction schemes, and to assess the fault-tolerance of the device.

- EC - FP6
- STREP

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